Remarks/Arguments

Claims 1-9 are pending. Claim 1 has been amended to more clearly and distinctly recite the subject matter that applicants regard as their invention. No new matter is believed to be added by the amendment.

Responsive to the objection to claim 5, the claim has been rewritten as an independent apparatus claim.

Responsive to the rejection of claims 8 and 9 under 35 USC 112, second paragraph, the claims have been amended to depend from claim 5.

Rejection of claims 1-8 under 35 USC 103(a) as being unpatentable over Isaka (US Pat. No. 5,740,373) in view of Adachi et al. (US Pat. No. 6,115,425).

Applicants submit that for the reasons discussed below present claims 1-8 are patentably distinguishable over the combination of Isaka and Adachi.

The examiner asserts that Isaka differs from the claimed invention in that Isaka does not specifically teach the step of carrying out a modulo-n counting of the data blocks in order to determine the data source packet boundaries, and in that the beginning of a new data source packet is signaled to a memory management device at the beginning of the next counting interval. Applicants submit that as discussed below Isaka also fails to teach other elements of the claimed invention.

Present claim 1 recites: "... receiving data transmitted in bus packets having a variable length, **each bus packet having a header and a payload data field, the payload data field being divided into data blocks having a defined length,** a combination of a defined number n of data blocks forming a data source packet of fixed length, section-by-section transmission of the data source packet within the framework of data blocks being permitted..." (emphasis added)

The Examiner asserts that Isaka teaches "... receiving data transmitted ... within the framework of data blocks being permitted" and cites col. 4, lines 29-44, col. 5, lines 25-31, and Fig. 7 in support of the assertion. Applicants respectfully submit that the cited portions of Isaka fail to teach the above-noted feature of claim 1.

In col. 5, lines 25-11, it is explained that the embodiment includes packet transmission circuitry for producing cells of fixed length from data of variable length and sequentially outputting them to the transmit bus 109. The embodiment disclosed by Isaka is in the context of an ATM network. As is well known by those skilled in the art, an ATM network is a cell based network, wherein all the data is sent in **fixed length cells**. The complete bus time is divided for fixed length cells. The cell of an ATM network corresponds to a bus packet because each cell has a header that contains the address information required for transferring the cell through the network. The header portion is followed by a data payload portion.

In view of the above, Applicants submit that it is incorrect and inappropriate to interpret a grouping of a particular number of ATM cells as corresponding to the bus packet having variable length recited in the present claims. In fact, Isaka teaches away from the present invention because the ATM network uses fixed length cells, each cell having a header portion and a payload portion.

Furthermore, in an ATM network, the problem of reconstructing the source packets from a variable section-by-section transmission of a fixed length source packet within data blocks does not exist. This is due to the fact that a variable length source packet will be sent in fractions of cells and a cell is a bus packet in the ATM system. Therefore, a bust packet having a variable length of data blocks from the source packet, such as that shown in Fig. 1 of the present application does not exist.

Also, the leading cell and the trailing cell of a source packet is specifically signaled in the cell header as disclosed in col. 4, line 57-60 of Isaka.

Adachi is cited as teaching the step of carrying out a modulo-n counting of the data blocks to determine the data source packet boundaries. Applicants respectfully submit that there is nothing in Adachi to suggest a modulo-N counting of fixed length data blocks for the purpose of finding the source packet boundaries of a source packet consisting of a fixed number of fixed length data blocks.

Adachi relates to a variable length coded data transmission device for use in a block encoder/decoder. The variable length blocks shown in Fig. 2 are distributed over fixed length slots, where the beginning of a variable length block is always at the beginning of a fixed length data slot. When a variable length data

block has data for more than a fixed length data slot, the remaining data will be distributed over the following fixed length data slots having unoccupied data capacity.

This is done in a manner that the data of an ith variable length block is started to fill in the ith slot. If all of the data of the variable length block does not fit in the ith slot, the remaining portion of the block is shifted to some unoccupied space of the next slot provided that there is some unoccupied space in the slot. Otherwise the slot following the next slot will be filled, etc. The method implies that in some of the N slots there is some unoccupied space.

In the present invention, the modulo-n counting is used for determining data source packet boundaries. Adachi is not concerned with data source packet boundary determination. Nowhere does Adachi teach or suggest that the variable length data block is divided in fixed length blocks. Nowhere does Adachi teach or suggest that variable length packets divided in fixed length blocks will be transmitted over a serial bus in bus packets of variable length in units of the fixed length data blocks.

In view of the above, applicants submit that the combination of Isaka and Adachi fail to teach or suggest all of the limitations of claim 1, and as such, claim 1, and the claims that depend therefrom, are patentably distinguishable over the cited combination.

Having fully addressed the Examiner's rejections, Applicants submit that the present application is in condition for allowance and respectfully request such action. No fee is believed due in regard to the present amendment. However, if a fee is due, please charge the fee to Deposit Account 07-0832. Should any questions arise regarding any of the above, the Examiner is requested to contact the undersigned at 609-734-6815.

Respectfully submitted,

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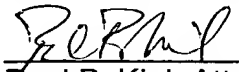
Siegfried Schweidler et al.

By: 

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